UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/410,504	10/01/1999	JAMES HEDLEY WILKINSON	450110-02215	6958

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20999	7590	06/24/2004	CZEKAJ, DAVID J

FROMMER LAWRENCE & HAUG
745 FIFTH AVENUE- 10TH FL.
NEW YORK, NY 10151

ART UNIT	PAPER NUMBER
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DATE MAILED: 06/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _28 May 2004_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-42_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-42_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _01 October 1999_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments with respect to claims 1-42 have been considered but are

moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

2.   Claims 1, 25, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Fujii et al. (5966385), (hereinafter referred to as "Fujii") in view of Eidson

(6278710).

Regarding claims 1 and 25, Fujii discloses an apparatus that filters TS

packets multiplexed with a plurality of programs and sends the filtered packets to

a decoder. This apparatus comprises an encoder that comprises a "clock and

means for deriving timing information relating to the digital signal from the clock"

(Fujii: column 1, lines 14-23, column 2, lines 1-4, wherein the timing information

is the PCR value). The data signal further comprises "data blocks, each data

block including a header containing data relating to the block and a plurality of

slots, each slot having a slot header relating to the slot and data packet" (Fujii:

column 1, lines 14-23 and 63-64, figure 3A, wherein the data blocks are formed

from a coding procedure and the data blocks are contained in the TS packet and

payload, column 2, lines 5-22 and figure 3B, wherein the PES packet is the slot,

the PES header is the slot header, and the data packet is the program element),

"plurality of data packets containing a first part and subsequent parts of the

signal" (Fujii: column 2, lines 1-22, figures 3A-3B, wherein the data packet is the

program element), "a first slot including the first part of the signal and a reference

time defining the time of production of the first part and each subsequent slot

containing a subsequent part of the signal and timing information defining a time

relative to a reference time" (Fujii: column 2, lines 1-22, figures 3A-B, wherein

the PES packet is the slot, the time information is the PCR and system clock),

and "means configured to derive from the clock a reference time defining the time

of production of the first part, the timing information defines the times of

productions of the subsequent parts" (Fujii: column 2, lines 1-22, figures 3A-3B,

wherein Fujii discloses using the PCR values to obtain the system or reference

clock which defines the whole packet consisting of the first and subsequent

parts). However, this apparatus lacks providing timing information of each

packet relative to other packets as claimed. Eidson teaches that reducing jitter

can be accomplished by ignoring packets that have a delay greater than a

minimum determined delay, wherein the delay is calculated by comparing the

timing data between packets (Eidson: column 5, lines 45-65). Therefore, it

would have been obvious to one having ordinary skill in the art at the time the

invention was made to take the apparatus disclosed by Fujii and add the timing

information between packets taught by Eidson in order to obtain an apparatus

that minimizes jitter.

Regarding claim 34, Fujii discloses that the "slots of each block are of

fixed length and have predetermined positions in the block" (Fujii: column 1,

lines 60-65 and figures 3A-B, wherein the slots of the block have a fixed size of

188 bytes and have a position show in figures 3A-B).

1.   Claims 2-8 and 26-33 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Fujii et al. (5966385), (hereinafter referred to as "Fujii") in view of Eidson (6278710)

in further view of O'Grady (6195392).

Regarding claims 2 and 26, note the examiners rejection for claims 1 and

25, and in addition, claims 2 and 26 differ from claims 1 and 25 in that claims 2

and 26 further require coarse and fine timing information. O'Grady teaches that

current methods of generating PCR's contain expensive components. O'Grady

discloses an apparatus that eliminates the need for these expensive components

presently necessary in the state of the art PCR generators (O'Grady: column 1,

line 66 to column 2, line 9). This apparatus comprises producing "coarse timing

info" (O'Grady: column 6, lines 30-48, wherein the coarse timing info is the result

of the pixel frequency dividing by an integer m) and "fine timing info" (wherein the

fine timing info is the program clock reference value base and extension).

Therefore, it would have been obvious to one having ordinary skill in the art at

the time the invention was made to take the apparatus disclosed by Fujii, add the

timing information between packets taught by Eidson, and add the PCR

generation method taught by O'Grady in order to obtain an apparatus that cost effectively encodes timing information into data blocks.

Regarding claim 3, O'Grady discloses an apparatus that receives "a clock signal, a modulo n counter which counts the clock signal and divides the clock signal frequency by n to produce the fine time information and a modulo m counter which counts the frequency divided clock signal produced by the modulo n counter, to produce the coarse time information" (O'Grady: column 6, lines 30-48 and figure 3, wherein the coarse timing info is the result of the pixel frequency dividing by an integer m and the fine timing info is the program clock reference value base and extension). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add the PCR generation specifics, i.e. the modulo counters, to obtain an apparatus that cost effectively encodes timing information into data blocks and help better synchronize that data.

Regarding claim 4, Fujii discloses "the clock signal frequency is 2.25n Mhz, where n is an integer" (Fujii: column 13, lines 26-27, wherein the clock signal frequency is 27 MHz which would correspond to an n integer value of 12).

Regarding claims 5-6, the specific values of the counters recited (12, 16, and 65536) would have been obvious variations in order to tweak the reference time so that the reference timing is closer to that of the TS program clock reference.

Regarding claim 7, Fujii discloses "a multiplexer for inserting the time information in the slots" (Fujii: column 1, lines 9-13).

Regarding claims 8 and 28, Fujii discloses "a means for inserting into the slot header a flag indicating whether the slot contains a first packet" (Fujii: column 2, lines 18-22, wherein the slot is the PES and the flag is the stream ID. Note, the stream ID indicates the element contents. If the stream ID contained no information, the PES would not contain a packet).

Regarding claim 27, O'Grady discloses that the "coarse and fine timing information are represented by separate words in the slot header" (O'Grady: column 1, lines 16-27, wherein the separate words are the set of flags that indicate the presence of optional fields such as PCR). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add the separate words in the slot header in order to better distinguish between the coarse and fine timing information.

Regarding claim 29, Fujii discloses a slot or PES header that "includes data indicating packet type" (Fujii: column 2, lines 9-12).

Regarding claim 30, Fujii discloses "data indicating packet type indicates one or both of packet length" (Fujii: column 2, lines 9-12, wherein packet length is the PES packet length).

Regarding claims 31 and 33, Fujii discloses packets that "include error correction data" (Fujii: column 2, lines 18-22, wherein the error correction data is CRC).

Regarding claim 32, Fujii discloses a slot or PES header that "includes
data indication whether or not the slot contains error correction data" (Fujii:
column 2, lines 9-12, wherein the "data indicator" is contained in other pieces of
information).

2.   Claims 16-23 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable
over Fujii et al. (5966385), (hereinafter referred to as "Fujii"), in view of Eidson
(6278710) in further view of Lenihan et al. (6169843), (hereinafter referred to as
"Lenihan") and O'Grady (6195392).

Regarding claims 16 and 17, note the examiners rejection for claims 1 and
25 and in addition Fujii discloses substantially the same encoder as above further
including a decoder that has "means for detecting the timing information of the
packets" (Fujii: column 2, lines 1-5). However claims 16 and 17 differ from
claims 1 and 25 in that claims 16 and 17 further require Fujii clock setting means
and comparing means and the coarse and fine timing information. Lenihan
teaches that a decoder can remove or ignore any null packets in incoming
transport streams such that only valid packets are made available (Lenihan:
column 7, lines 25-28). Lenihan discloses an apparatus that can generate or set
the a time at which the packet was received relative to a system time clock
(Lenihan: column 7, lines 35-38) and compare and output the times when the
times are equal to a certain value (Lenihan: column 12, lines 9-25). O'Grady
teaches that current methods of generating PCR's contain expensive
components. O'Grady discloses an apparatus that eliminates the need for these

expensive components presently necessary in the state of the art PCR

generators (O'Grady: columns 1-2, lines 66-9). This apparatus comprises

producing "coarse timing info" (O'Grady: column 6, lines 30-48, wherein the

coarse timing info is the result of the pixel frequency dividing by an integer m)

and "fine timing info" (wherein the fine timing info is the program clock reference

value base and extension). Therefore, it would have been obvious to one having

ordinary skill in the art at the time the invention was made to take the apparatus

disclosed by Fujii, add the timing information between packets taught by Eidson,

add the decoder taught by Lenihan, and add the timing information taught by

O'Grady in order to have the best control means possible over the transport

streams.

Regarding claim 18, O'Grady discloses an apparatus that receives "a

clock signal, a modulo n counter which counts the clock signal and divides the

clock signal frequency by n to produce the fine time information and a modulo m

counter which counts the frequency divided clock signal produced by the modulo

n counter, to produce the coarse time information" (O'Grady: column 6, lines 30-

48 and figure 3, wherein the coarse timing info is the result of the pixel frequency

dividing by an integer m and the fine timing info is the program clock reference

value base and extension). Therefore, it would have been obvious to one having

ordinary skill in the art at the time the invention was made to add the PCR

generation specifics, i.e. the modulo counters, to obtain an apparatus that cost

effectively encodes timing information into data blocks and help better
synchronize that data.

Regarding claim 19, Fujii discloses "the clock signal frequency is 2.25n
Mhz, where n is an integer" (Fujii: column 13, lines 26-27, wherein the clock
signal frequency is 27 MHz which would correspond to an n integer value of 12).

Regarding claims 20-21, the specific values of the counters recited (12,
16, and 65536) would have been obvious variations in order to tweak the
reference time so that the reference timing is closer to that of the TS program
clock reference.

Regarding claim 22, Fujii discloses "a decoder for use with a signal the
slot header of which contains a flag indicating whether the slot contains a said
first packet, the decoder comprising a demultiplexer for separating the flag and
the packet, and means responsive to the flag for setting the clock to the
reference time if the flag indicates a first packet" (Fujii: column 2, lines 5-12.
column 12, lines 1-43, and figure 18 wherein the slot header is the PES header,
the flag is the stream ID, the demultiplexer is the channel demultiplexer, and the
means for setting the clock is carried out by the error flag delay circuit).

Regarding claim 23, Lenihan discloses that the "outputting means
comprises a FIFO buffer" (Lenihan: figure 3A, items 316, 335, and 355).
Therefore, it would have been obvious to one having ordinary skill in the art at
the time the invention was made to add the FIFO buffer in order to obtain a
method for outputting the packets at a desired time.

3.   Claims 9-15 and 35-42 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Fujii et al. (5966385), (hereinafter referred to as "Fujii") in view of

Eidson (6278710) in further view of Hurst et al. (6141358), (hereinafter referred to as

"Hurst").

        Regarding claim 9, note the examiners rejection for claims 1 and 25 and

in addition, claim 9 differs from claims 1 and 25 in that claim 9 further requires

variable length data blocks. Hurst teaches that blocks of data do not need to be

evenly distributed or of similar size in order to be transported within an SDTI

system (Hurst: column 3, lines 62-64, wherein the chunks are the blocks of

data). Therefore, it would have been obvious to one having ordinary skill in the

art at the time the invention was made to take the apparatus disclosed by Fujii,

add the timing information between packets taught by Eidson, and add the

variable length blocks taught by Hurst in order to obtain a more efficient

transporting means.

        Regarding claims 10 and 36, Fujii discloses "said slots are variable length

slots" (Fujii: column 2, lines 5-7, wherein the slot is the PES packet and the

variable length slot is the variable length packet).

        Regarding claims 11 and 37, Fujii discloses "variable length slots that

comprise slots containing metadata and slots containing data described by the

metadata" (Fujii: column 2, lines 18-22 and figure 3B, wherein the metadata is

the section header).

Regarding claims 12 and 38, note Fujii, figure 3B. The metadata slot "precedes the data slots containing the data described by the metadata" (wherein the metadata slot is the section header).

Regarding claims 13 and 39, note Fujii figure 3B. The metadata slot "contains metadata identifying a succeeding slot which contains a said first packet" (wherein the metadata slot is the section header).

Regarding claim 14 and 40, Fujii discloses "variable length slots that comprise a data field, a type field containing data describing the type of data in the data field, and a length field defining the length of the data in the data field (Fujii: column 2, lines 5-24, wherein the data field is the PES packet, the type field is the PES header, and the length field is the time stamp information (PTS)).

Regarding claim 15, Hurst discloses a serial data transport (SDTI) bitstream data structure carrying an MPEG information sub-stream (Hurst: figure 2). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add the SDTI to the encoder in order to allow the blocks to be placed on the high bitrate information stream.

Regarding claim 35, Hurst discloses data blocks are "variable length blocks" (Hurst: column 3, lines 62-64, wherein the variable length blocks are chunks that do not need to be similar in size). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add the variable length data blocks in order to accommodate data of varying size.

Regarding claim 41, Hurst discloses that "blocks and block headers conform to SDTI" (Hurst: column 8, lines 62-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to ensure the blocks conform to SDTI in order to allow the blocks to be placed on the high bitrate information stream.

Regarding claim 42, Hurst discloses that the "said packets are MPEG 2 TS packets" (Hurst: column 3, lines 40-41). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to make the packets MPEG2 TS packets in order to comply with the MPEG standards.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dave Czekaj whose telephone number is (703) 305-3418. The examiner can normally be reached on Monday - Friday 9 hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on (703) 305-4856. The fax phone number for the organization where this application or proceeding is assigned is (703) 872 9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

CHRIS KELLEY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600